

## SCC details

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Supporting the audio and video inputs and outputs, the SCC described by Toshiba at Hot Chips has an architecture optimized to deliver a high quality of service. It handles resource bandwidth allocation via a bus arbitration mechanism with priority in every cycle (Fig. 3). Internally, it employs two buses. One processes video and audio streams in real time and the other handles "best-effort" processing for data movement to storage and I/O ports, such as USB and Gigabit Ethernet interfaces.

The chip also includes management logic to prevent conflicts between or among operating systems, and it provides content security via a hardware random number generator and multiple encryption/decryption provisions. The SCC includes a DDR2 DRAM interface for video RAM, with a dedicated DMA controller for streaming data. Also on the chip are high-definition and standard-definition video and audio inputs and outputs, an IEEE 1394 (FireWire) interface for connecting digital A/V equipment, and a transport stream interface for a digital tuner. Connectivity options include PCI, PCI-Express, and USB 2.0, a Gigabit Ethernet high-speed network interface, and a parallel ATA interface for connecting storage devices.

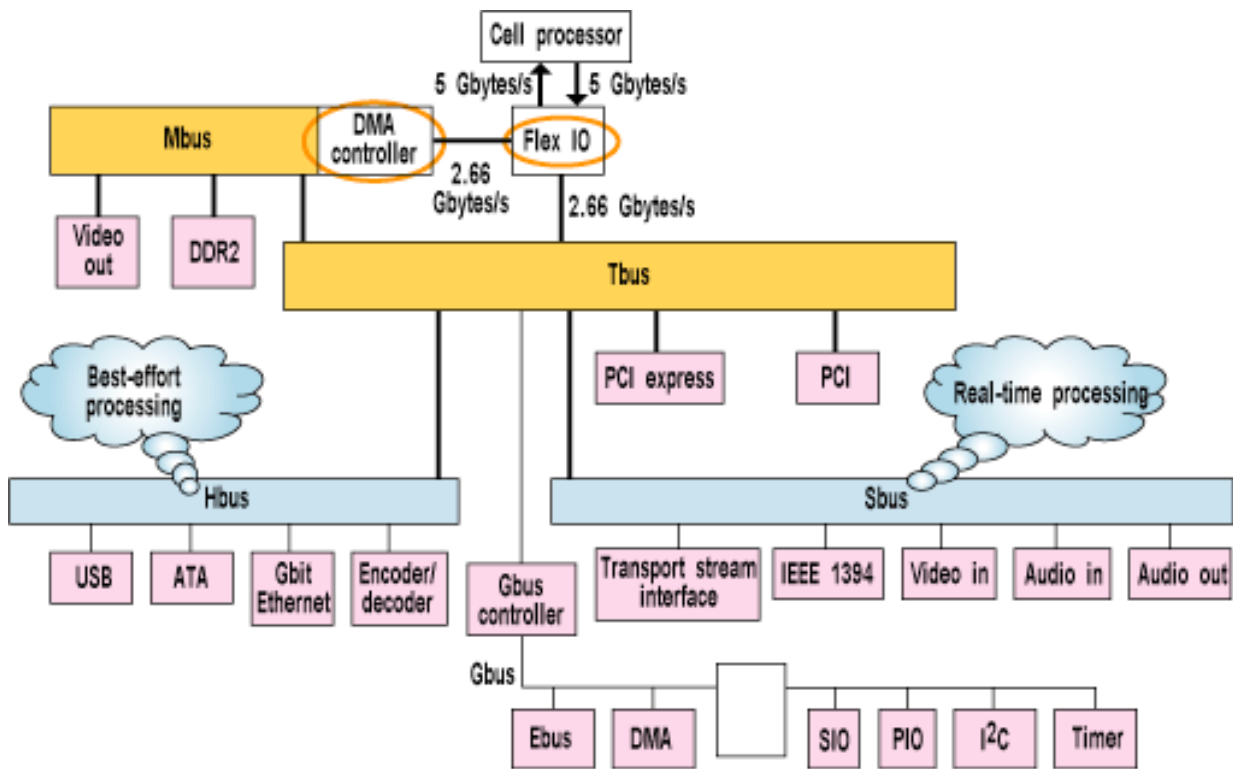
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## Toshiba Unveils I/O processor LSI for Cell

Toshiba Corp. has developed "Super Companion Chip (SCC)," an LSI for input-output interface processing to be used with the microprocessor "Cell", and presented it at the international academic conference "A Symposium on High Performance Chips (HOT CHIPS) 17." It works as a relay when the Cell processes signals compliant with G-bit Ethernet and IEEE1394 or those used in the digital terrestrial broadcasting. It is the first time that Toshiba presents the SCC at an academic conference. Although the release date is yet to be disclosed, the company expects to start the volume production by the second half of 2005. The target application is AV equipment such as a digital TV receiver.

The data transmission between the SCC and the Cell is performed by using FlexIO with the maximum data transfer rate of 5 Gbytes per second. Both upload and download traffics have a bandwidth of 5 Gbytes per second. The CSS includes the interface circuits which support the DDR2-compliant DRAM, video input-output, IEEE1394, PCI and PCI Express, USB 2.0, G-bit Ethernet, Ultra ATA/133 and others. The interfaces for USB 2.0, G-bit Ethernet and Ultra ATA/133 are the best-effort connection using an internal bus, while those for the IEEE1394, video input-output and transport stream are the bandwidth-guaranteed connection using the internal bus.

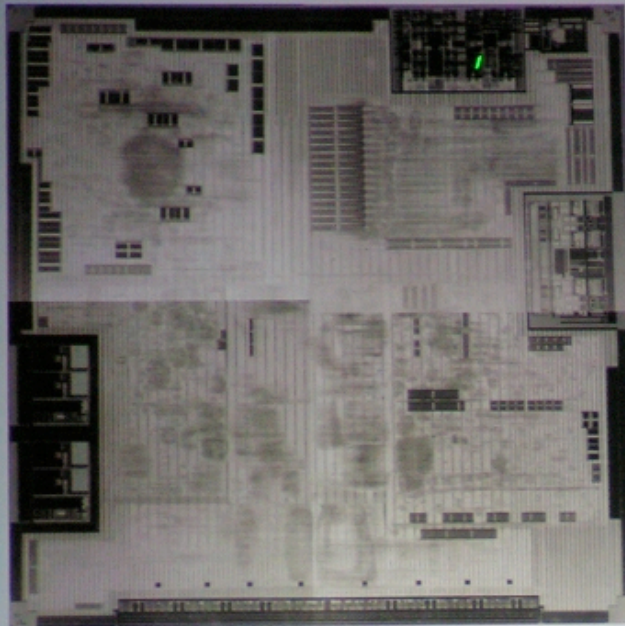
Toshiba presented a photo of a prototype chip at the HOT CHIPS. It is a seven-layered Cu-wired chip measuring 12.71 x 12.71 mm that utilizes 90-nm CMOS technology. The maximum operating frequency is 333 MHz, and the core voltage supply of  $\pm 1.2$  V is required. The chip is packaged in a 1385-terminal PBGA package.



3. All the I/O support for the Sony Playstation 3 game system will be handled by this super companion chip developed by Toshiba. It interfaces to the jointly developed Cell Processor and handles audio, video inputs and outputs, as well as data interfaces to USB, Gigabit Ethernet, and storage ports.

**TOSHIBA**

## Chip Photo



- **Process**  
90nm CMOS Process  
7 Layer Cu
- **Frequency**  
-333MHz
- **Package**  
PBGA[FC], 1385pin,  
40mm□, 1mm pitch
- **Chip Size**  
12.71mm x 12.71mm
- **VDD**  
Core: 1.2V  
I/O: Multiple voltages for  
various peripherals